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CLAIMS

What is claimed is:

1. An automated method for designing integrated circuits (ICs), comprising the steps of:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block; and

generating at least one design-specific cell representative of said functional block, said design-specific cell generated based on said design objective of said IC.

2. The method of claim 1, wherein said step of generating comprises evaluating said design-specific cell based on the context in which said design-specific cell is to be used.

3. The method of claim 1, wherein said step of generating comprises characterizing and selecting said design-specific cell from a minimal set of at least one cell based on said IC design objective.

4. The method of claim 3, wherein said step of characterizing and selecting is repeated until the design-specific objective is met.

5. The method of claim 1, wherein said design objective is selected from the group consisting of: IC design die size (area), performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability and cost.

6. The method of claim 1, further comprising a step of optimizing said IC design.

7. The method of claim 6, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

8. The method of claim 6, wherein said step of optimizing is performed automatically.

9. The method of claim 8, wherein said step of optimizing is repeated until said IC design meets at least one optimization metric.

10. The method of claim 1, wherein said design-specific cell is a transistor-level cell.

11. A system for implementing an automated integrated circuit (IC) design process, said system comprising:

a means for describing said IC, said description including at least one design objective of said IC;

a local optimization control for partitioning said description into at least one functional block; and

a design-specific cell generation means for generating at least one design-specific cell representation of the functional block, said design-specific cell generated based on said design objective of said IC.

12. The system of claim 11, further comprising a means for evaluating said design-specific cell based in the context in which said design-specific cell is to be used.

13. The system of claim 11, further comprising means for characterizing and selecting said design-specific cell from a minimal set of at least one cell based on said IC design objective.

14. The system of claim 13, wherein said means for characterizing and selecting is repeated until said design-specific objective is satisfied.

15. The system of claim 11, wherein said design-specific cell generation means selects said design objective from a group consisting of: IC design die size (area), performance, power consumption, routability, fault tolerance, signal integrity, testability, reliability, and cost.

16. The system of claim 11, further comprising means for optimizing said IC design.

17. The system of claim 16, wherein a criteria used by said means for optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

18. The system of claim 16, wherein said means for optimizing is performed automatically.

19. The system of claim 16, wherein said means for optimizing is iteratively optimized until said IC design meets at least one optimization metric.

20. The system of claim 11, wherein said design-specific cell generation means is capable of generating a transistor-level design-specific cell.

21. A design-specific cell produced by an automated IC design process, said IC design process comprising:

describing the IC, the description including at least one design objective of said IC;

partitioning said description into at least one functional block; and

generating at least one design-specific cell representative of said the functional block, said design-specific cell generated based on the design objective of said IC.

22. The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises evaluating said design-specific cell based on the context in which said design-specific cell is to be used.

23. The design-specific cell produced by said IC design process of claim 21, wherein said IC design process characterizes and selects said design-specific cell from a minimal set of at least one design-specific cell based on said IC design objective.

24. The design-specific cell produced by said IC design process of claim 23, wherein said IC design process characterizing and selecting is repeated until said design-specific objective is met.

25. The design-specific cell produced by said IC design process of claim 21, wherein said design objective of said IC design process is selected from the group consisting of: IC design die size (area), performance, power consumption, signal integrity, routability, fault tolerance, testability, reliability, and cost.

26. The design-specific cell produced by said IC design process of claim 21, wherein said IC design process further comprises a step of optimizing said IC design.

27. The design-specific cell produced by said IC design process of claim 26, wherein a criteria for said step of optimizing is selected from the group consisting of: clock speed, transistor sizing, number of transistors, power consumption, fault tolerance, signal integrity characteristics, noise characteristics, and a combination thereof.

28. The design-specific cell produced by said IC design process of claim 21, wherein said step of optimizing is performed automatically.

29. The design-specific cell produced by said IC design process of claim 28, wherein said step of optimizing is repeated until said IC design satisfies at least one optimization metric.

30. A storage medium having computer readable program instructions embodied therein for automatically designing an integrated circuit (IC), said storage medium comprising:

program instructions for describing the IC, the description including at least one design objective of said IC;

program instructions for partitioning said description into at least one functional block; and

program instructions for generating at least one design-specific cell representative of the functional block, said design-specific cell generated based on the design objective of said IC.